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10/668,166	09/24/2003	Toshio Kimura	1035-473	4031
23117 7590 07/02/2007 NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			EXAMINER ARENA, ANDREW OWENS	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Claim Objections

Claim 8 is objected to because the recitation "a number of adjacent connected ones of the through electrodes which are connected to either a ground..." is unclear and renders the claim indefinite. It is clear from applicant's specification and other claims that this recitation is intended to convey that the adjacent electrodes are connected to each other, however, the claim does not necessarily read this way. The language is confusing because it may simply require that more electrodes are connected to either ground or power than a particular signal.

Claim 8 will be interpreted as claims 1 and 7, but clarification is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 4, 5, 7, 8, 9, 11, 12, 13, 15, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumikawa (US 6,362,529) in view of Anderson (US 6,661,100).

Re claim 1, Sumikawa discloses (Figs 3, 6, 7; col 5 ln 20-41) a semiconductor device comprising (referring to Fig 3):

a plurality of spaced apart through electrodes (2; col 3 ln 32) with equal cross sectional areas in a semiconductor chip (1; col 3 ln 30) which through electrodes

electrically link a front surface of the chip to a back surface of the chip (col 3 ln 38-40),
wherein

a least one of the plurality of through electrodes is in communication with a
power supply (inherent; this must be true in order to operate the chip),

at least another one of the plurality of through electrodes is in communication
with ground (inherent; this must be true in order to operate the chip),

at particular signal-routing through electrode is formed of only one of the plurality
of through electrodes (e.g., 22a in Fig 4; col 4 ln 53); and

at least one of the plurality of through electrodes is a non-contact through
electrode which is electrically isolated from the chip (col 4 ln 3-6; col 4 ln 45-55).

Sumikawa differs from the claimed invention only in not disclosing a plurality of
through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5;
Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a
semiconductor chip (200) wherein at least two electrodes are connected to one another
to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least
another electrodes are connected to one another to form a second high-current
electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing
electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of
ordinary skill instantly appreciates that connecting a plurality of electrodes increases the
effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply and at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground; at least to reduce power losses.

Re claim 2, Sumikawa discloses at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip (col 4 ln 53-55).

Re claim 4, the combined device discloses both of the first number and the second number is two or greater (Anderson: Fig 2), so that each of the first (210) and second (220) high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode (205) is made up of only one of the through electrodes.

Re claim 5, Sumikawa discloses multiple stacked semiconductor chips, each of the semiconductor chips including a semiconductor device according to claim 1.

Re claim 7, Sumikawa discloses (Figs 3, 4, 6, 7; col 5 ln 20-41) a chip-stack semiconductor device comprising:

a plurality (Fig 4) of stacked semiconductor chips (1, 21; col 4 ln 21-22), each of the semiconductor chips including a plurality of through electrodes (2, 22; col 4 ln 36) with equal cross-sectional areas therein linking a front surface to a back surface thereof,

wherein at least one first high-current electrode is connected to a power supply and at least one second high-current electrode is connected to ground (inherent; this must be true in order to operate the chip), and a signal-routing electrode connecting a front [surface to] a back surface of one of the semiconductor chips is made up of only one of the through electrodes (e.g., 22a in Fig 4; col 4 ln 53), and

at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip (col 4 ln 3-6; col 4 ln 45-55).

Sumikawa differs from the claimed invention only in not disclosing a plurality of through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5; Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a semiconductor chip (200) wherein at least two electrodes are connected to one another to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least another electrodes are connected to one another to form a second high-current electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of ordinary skill instantly appreciates that connecting a plurality of electrodes increases the effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least one of a first high-current through electrode connected to a power supply and a second high-current through

electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another; at least to reduce power losses.

Re claim 8, Sumikawa discloses (Figs 3, 4, 6, 7; col 5 ln 20-41) a chip-stack semiconductor device comprising:

multiple stacked (Fig 4) semiconductor chips (1, 21; col 4 ln 21-22), each of the semiconductor chips including a number of through electrodes (2, 22; col 4 ln 36) with equal cross-sectional areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined (no implied structure: MPEP 2114) in accordance with a magnitude of an electric current to be conducted therethrough, wherein

a number of through electrodes are connected to [a] either a ground terminal or a power supply terminal of that semiconductor chip (inherent; this must be true in order to operate the chip) and a number of through electrodes are connected to a particular signal terminal (e.g., 22a in Fig 4; col 4 ln 53), and

at least one of the through electrodes is a non-contact through electrode which is electrically isolated from the semiconductor chip in which it is formed (col 4 ln 3-6; col 4 ln 45-55).

Sumikawa differs from the claimed invention only in not disclosing a plurality of through electrodes connected to one another to form a high-current through electrode.

Anderson discloses an analogous stacked-chip semiconductor device (col 3 ln 5; Fig 3) comprising (Fig 2) a plurality of spaced apart electrodes (205) on a

semiconductor chip (200) wherein at least two electrodes are connected to one another to form a first high-current electrode (210) for power supply (VDD; col 4 ln 8-12), at least another electrodes are connected to one another to form a second high-current electrode (220) for ground supply (GND; col 4 ln 3-7), and a particular signal-routing electrode (205) is formed of only one electrode.

It is fundamental in electrical arts that resistance is proportional to area; one of ordinary skill instantly appreciates that connecting a plurality of electrodes increases the effective cross-sectional area of the conductor and carries a given signal with less loss.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Anderson, at least one of a first high-current through electrode connected to a power supply and a second high-current through electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another; at least to reduce power losses.

Re claims 9, 11, & 12, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent; e.g., Sumikawa Fig 4).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes used in connecting different numbers of chips.

It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that a number of those through electrodes which connect $n+1$ or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2; at least to reduce impedance.

Re claims 13, 15, & 16, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent; e.g., Sumikawa Fig 4).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased with interconnect line length.

It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased; at least to reduce impedance.

Furthermore, the recitation "is increased as..." is not a structural limitation but seems to be either a recitation of indented use or manner of operating; such recitations do not impart patentability to apparatus claims such as these. See MPEP § 2114.

Re claims 17, 19, & 20, the combined device discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent; e.g., Sumikawa Fig 4).

Sumikawa as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased in proportion to an interconnect line length.

It is well known that a larger total conductor cross-section is used for a proportionally longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips; at least to reduce impedance.

Furthermore, the recitation "is increased as..." is not a structural limitation but seems to be either a recitation of indented use or manner of operating; such recitations do not impart patentability to apparatus claims such as these. See MPEP § 2114.

Response to Arguments

Applicant's arguments filed 03/07/2007 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Sumikawa.

Although Hayasaka seems to suggest non-contact through electrodes, the suggestion is not conclusive enough to support the previously applied rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure in disclosing stacked-chips with through electrodes, however, those references not relied upon do not seem to expressly disclose non-contact through electrodes as required by the currently pending claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Andrew O Arena
25 June 2007


Sara Crane
Primary Examiner